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10/757,928	01/15/2004	Joseph Huang	ALTR:023	6328

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EXAMINER	
WEINBERG, MICHAEL J	

ART UNIT	PAPER NUMBER
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,928	HUANG ET AL.	
	Examiner	Art Unit	
	Michael J. Weinberg	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-17* is/are allowed.

6)☒ Claim(s) *1-8 and 18-52* is/are rejected.

7)☐ Claim(s) *1-8,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendments were filed on 7/20/2006 and 8/5/2006. The new drawings are acceptable. Claims 1, 5-9, 18, 23-26, 30, and 41 are amended. Claims 1-52 are pending.

2. Applicant's arguments with respect to the claims, as amended, have been considered but are moot in view of the new ground(s) of rejection. The new rejections, were necessitated by the amendment.

3. In addition, it is noted that claim 1 recites "decoder circuitry coupled to a set of storage circuits". However, as broadly recited, "storage circuits" could mean the fuses or the circuit blocks/memory cells that are being replaced. Though the claims are rejected below on more substantial grounds, this is one additional reason why the claims will need to be amended.

4. Lastly, the examiner believes that there may be aspects of Applicant's invention that are novel and not obvious. However, these aspects are not currently reflected in all of the claims. See "Allowable Subject Matter" below for details.

Claim Objections

5. Claims 1-8 and 33-34 are objected to because of the following informalities:

With regard to **claim 1, associated depending claims, and claim 33**, it has been held that the recitation that an element is **"adapted to"** perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Huchison, 69 USPQ 138.*

Claims 34-38 are objected to because the limitations of claim 34 are already recited in claim 30.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-6 and 18-27, 29, 30, 34, 35, and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Anand et al (US Patent 6,552,938).

With regard to **claim 1**, Anand discloses an integrated circuit (IC) including redundancy circuitry 18 (see figures 1b and 1c) configured to provide redundancy by using a decoder circuitry 28 coupled to a set of storage circuits (24, 26), wherein the decoder circuitry 28 is configured to decode coded defect information received from a set of circuit elements 12 adapted to provide the coded defect information. (see col. 5, for example)

With regard to **claim 2**, Anand discloses an integrated circuit (IC) according to claim 1, wherein the redundancy circuitry is further configured to provide redundancy by

bypassing a defective circuit block within the integrated circuit (IC). (As in the abstract, Anand provides redundancy for a data line--ie a column--of a memory. Column 3, lines 15-40 detail that individual blocks have redundancy.)

With regard to **claim 3**, Anand discloses an integrated circuit (IC) according to claim 2, wherein the redundancy circuitry is further configured to provide redundancy by using a redundant circuit block to perform the functionality of the bypassed defective circuit block. (This is a column redundancy system as in the abstract. A column is a block of cells.)

With regard to **claim 4,** Anand discloses an integrated circuit (IC) according to claim 1, wherein the redundancy circuitry is further configured to provide redundancy for a plurality of circuit blocks within the integrated circuit (IC). (Col. 3, lines 15-24 show individual blocks of memory have redundancy and col. 6, lines 40-50 show multiple data lines have redundancy. Both may be interpreted as the blocks of the claims.)

With regard to **claim 5,** Anand discloses an integrated circuit (IC) according to claim 4, wherein the set of circuit elements comprise a plurality of programmable circuit elements. (fuses 12 in figures 2a and 2b)

With regard to **claim 6,** Anand discloses an integrated circuit (IC) according to claim 5, where in a number of the plurality of programmable circuit elements is smaller than the number of the circuit blocks in the plurality of circuit blocks. (see col. 3, lines 45-67 where it is taught that 4 bits are stored for 10 data lines)

With regard to **claim 18,** Anand discloses an programmable logic device (Note that the circuit of Anand can be interpreted broadly as programmable logic since the memory is programmable to a 1 or 0 and comprises logic circuits.), comprising:

a plurality of programmable elements 12, the plurality of programmable elements configured to provide a first set of signals (see line to decoder 28 and binary fuse data signal discussed in the last paragraph of col. 3);

a decoder circuit 28 coupled to the plurality of programmable elements 12, the decoder circuit 28 configured to derive a second set of signals (See lines from decoder to registers and ten-bit code discussed in the last paragraph of col. 3) from the first set of signals and to provide the second set of signals to a shift register 24; and

redundancy circuitry (30 and 18- see figures 1b and 1c) coupled to the decoder circuit, wherein

the redundancy circuitry is responsive to the second set of signals. (see abstract and figures 2a and 2b)

With regard to **claim 19,** Anand discloses a programmable logic device according to claim 18, wherein the first set of signals comprises a set of signals configured to identify a defective circuit in the programmable logic device (PLD). (abstract)

With regard to **claim 20,** Anand discloses a programmable logic device (PLD) according to claim 19, wherein the set of signals configured to identify the defective circuit comprises coded signals. (see col. 3, lines 45-67)

With regard to **claim 21,** Anand discloses a programmable logic device (PLD) according to claim 20, further comprising a redundant circuit (see figures 1a/1b), wherein, in response to the second set of signals, the redundancy circuitry causes an input signal to be coupled to the redundant circuit instead of the defective circuit. (see col. 4, lines 22-43)

With regard to **claim 22,** Anand discloses a programmable logic device (PLD) according to claim 21, wherein, in response to the second set of signals, the redundancy circuitry causes an output signal of the redundant circuit to be used instead of an output signal of the defective circuit. (see col. 4, lines 22-43 and col. 5)

With regard to **claim 23,** Anand discloses a programmable logic device (PLD) according to claim 22, wherein the coded signals correspond to information programmed in the programmable elements. (see col. 3, lines 45-67)

With regard to **claim 24,** Anand discloses a programmable logic device (PLD) according to claim 2318, wherein each of the programmable elements comprises a fuse 12. (see col. 3, lines 45-67)

With regard to **claim 27,** Anand discloses a programmable logic device (PLD) according to claim 22, wherein the defective circuit comprises a memory circuit, and wherein the redundant circuit comprises a memory circuit. (see abstract, first line)

With regard to **claim 29**, Anand discloses a programmable logic device (PLD) according to claim 22, wherein the defective circuit comprises programmable interconnect circuitry, and wherein the redundant circuit comprises programmable

interconnect circuitry. (figures 1a/1b show spare interconnect circuitry connected to the memory)

With regard to **claim 30,** Anand discloses a programmable logic device (PLD), comprising:

a first block of memory; (connected to normal lines in figures 1a/1b)

a plurality of programmable fuses (12 in figures 2a/2b), the plurality of programmable fuses configured to provide a set of coded (binary) signals corresponding to a defect in the first block of memory; (see last paragraph of col. 3)

a decoder circuit 28 configured to derive a decoded set of signals from the coded set of signals; (see last paragraph of col. 3)

a pluralitv of flip-flops (shift registers 24) coupled to the decoder circuit, the pluralitv of flip-flops configured to receive the decoded set of signals;

redundancy circuitry (24, 26, and 18 as shown in figures 1-2) coupled to the decoder circuit 28, the redundancy circuitry configured to respond to the decoded set of signals; and

a second block of memory (spare columns in figures 1a/1b) coupled to the redundancy circuitry 18, wherein

the second block of memory is used to provide redundancy for the first block of memory: (as in the abstract)

With regard to **claim 34**, Anand discloses a programmable logic device (PLD) according to claim 30, wherein the redundancy circuitry comprises a set of flip-flops 24 configured to receive the decoded set of signals from the decoder circuit.

With regard to **claim 35**, Anand discloses a programmable logic device (PLD) according to claim 34, wherein the redundancy circuitry further comprises a set of OR gates, wherein each OR gate in the set of OR gates couples to a respective flip-flop in the set of flip-flops. (see figures 3a-3b)

With regard to **claim 40**, Anand discloses a programmable logic device (PLD) according to claim 30, further comprising programmable interconnect circuitry coupled to the second memory block. (figures 1a/1b show spare interconnect circuitry connected to the memory)

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7, 8, 25, 26, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of Yamada (US Patent 4,747,080).

With regard to **claims 7, 8, 25, 26, 31, and 32**, Anand discloses an integrated circuit (IC) according to claim 5 and programmable logic devices (PLD) according to claims 18 and 30, but does not teach a particular type of fuse in use such as laser programmed or electrically programmed fuses.

However, Yamada does teach a device with redundancy wherein each of the programmable circuit elements (for storing an address of a defect) comprises an

electrically programmed fuse or laser-programmed fuse (column 13, lines 50-65), as is common in the art.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a laser-programmed or electrically programmed fuse in the invention of Anand in order to cheaply store the address of a defect.

10. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of Fuchigami (US Patent 6,219,286).

With regard to **claim 33**, Anand discloses the PLD of claim 30 but does not specifically teach the makeup of his decoder 28.

However, Fuchigami discloses a programmable logic device (PLD) with a decoder (see figure 12) comprising:

at least one inverter 121a-f adapted to receive coded signals; and

at least one AND gate (122a-f, 123a-f, 124a-f) coupled to the at least one inverter, wherein the at least one AND gate provides the decoded set of signals.

This type of decoder is not only well-known in the art but also the type that one of ordinary skill would use in order to implement the decoding discussed in the last paragraph of col. 3.

As such, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the well-known decoder as exemplified by Fuchigami in Anand in order to, for example, save design time by using common VLSI decoder models.

11. Claim 34-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of the Application Prior Art C6 "MRAM redundancy Scheme" (which will be further referred to as C6).

With regard to **claims 34-38**, Anand teaches the device of claim 30, but does not show the limitations of claims 36-38. However, with regard to **claim 34** (rejected again), C6 does teach a redundancy circuitry comprising a set of flip-flops configured to receive a decoded set of signals D[n] from a decoder circuit.

With regard to **claim 35** (rejected again), C6 teaches that the redundancy circuitry further comprises a set of OR gates, wherein each OR gate in the set of OR gates couples to a respective flip-flop in the set of flip-flops.

With regard to **claim 36**, C6 further teaches that the redundancy circuitry further comprises a set of multiplexers, wherein each multiplexer in the set of multiplexers couples to a respective OR gate in the set of OR gates.

With regard to **claim 37**, C6 further teaches a first multiplexer in the set of multiplexers couples to the first block of memory.

With regard to **claim 38**, C6 further teaches a second multiplexer in the set of multiplexers that couples to the second block of memory.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the device of Anand with the redundancy circuit of C6 in order to allow a switching away from defective cells to spare cells. There is expectation of success to combine the two references as the flipflops of Anand could control the circuitry of C6.

12. Claims 41-50 and 52 are are rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of the Admitted Prior Art.

Anand teaches a device (see 102 rejections above) that uses all of the steps of the methods of providing redundancy in an integrated circuit (IC) in claims 41-50 and 52 but he does not teach receiving a scan chain testing signal. Anand specifically teaches that testing occurs in col. 1, lines 20-25 and that redundancy data from the testing that must occur (je the limitations of claim 48) is stored in the fuses 12.

He does not disclose receiving a scan chain testing signal but, as said above. there must have been some sort of testing performed.

Paragraph 66 of the disclosure of Applicant teaches, "Scan chain testing allows the testing of circuitry within an IC. The details of scan chain testing fall within the knowledge of persons of ordinary skill in the art."

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to receive a scan chain testing signal (for example the type shown in APA C6) in order to test the IC and obtain the defective addressed.

13. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of APA and further in view of Kalter et al (US Patent 5,796,662).

With regard to **claim 51**, Anand and APA disclose a method according to claim 50 including providing a device which switches links 18 connected to blocks/columns of memory cells. Though he does not teach that the redundant circuitry comprises programmable logic circuitry, Anand does teach that Kalter is incorporated by reference and can be used in the column redundancy system. (see top of col. 4 of Anand)

Kalter teaches in figure 2, col. 4, lines 28-40 and col. 5, starting at line 33 that programmable logic arrays have been used with redundancy circuitry.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use programmable logic circuitry taught in Kalter with the redundancy system of Anand and APA in order to properly correct errors in programmable logic.

14. Claims 41-50 are rejected (again) under 35 U.S.C. 103(a) as being unpatentable over Fuchigami (from the previous office action) in view of the Admitted Prior Art.

With regard to **claim 41**, Fuchigami discloses a method of providing redundancy in an integrated circuit (IC), the method comprising:

retrieving information (from register unit 4) about a defect in the integrated circuit (IC), wherein the information about the defect is coded in the integrated circuit (abstract);

decoding (using decoder 31) the information about the defect to identify a defective circuit within the integrated circuit (abstract); and

using a redundant circuit (WL_{n+1} where n is the row number of the row with a defect) within the integrated circuit (IC) instead of the identified defective circuit WL_n (column 7, lines 1-7 and column 1, lines 57-61).

He does not disclose receiving a scan chain testing signal but, clearly, in order to determine the defective address, there must have been some sort of testing performed.

Paragraph 66 of the disclosure of Applicant teaches, "Scan chain testing allows the testing of circuitry within an IC. The details of scan chain testing fall within the knowledge of persons of ordinary skill in the art."

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to receive a scan chain testing signal (for example the type shown in APA C6) in order to test the IC and obtain the defective addressed.

With regard to **claim 42**, Fuchigami discloses a method according to claim 41, wherein retrieving information about a defect in the integrated circuit (IC) further comprises retrieving information coded in a set of programmable elements 4 within the integrated circuit (abstract).

With regard to **claim 43**, Fuchigami discloses a method according to claim 42, wherein decoding the information about the defect to identify a defective circuit within the integrated circuit (IC) further comprises generating a set of decoded signals (using decoder 31) from the information about the defect (abstract).

With regard to **claim 44**, Fuchigami discloses a method according to claim 43 (see figure 12), wherein the number of signals in the set of decoded signals (totaling 12) is larger than the number of programmable elements in the set of programmable elements (totaling 6).

With regard to **claim 45**, Fuchigami discloses a method according to claim 43, wherein using a redundant circuit within the integrated circuit (IC) instead of the identified defective circuit further comprises bypassing the identified defective circuit (abstract).

With regard to **claim 46**, Fuchigami discloses a method according to claim 43, wherein using a redundant circuit within the integrated circuit (IC) instead of the identified defective circuit further comprises routing (thanks to selection circuit group 33)

a set of input/output signals (through R_n) to the redundant circuit instead of the identified defective circuit (abstract).

With regard to **claim 47**, Fuchigami discloses a method according to claim 46, wherein routing (thanks to selection circuit group 33) a set of input/output signals to the redundant circuit instead of the identified defective circuit further comprises:

routing an input signal to the redundant circuit instead of the identified defective circuit; and

using an output signal of the redundant circuit instead of an output signal of the identified defective circuit (all in abstract).

With regard to **claim 48**, Fuchigami discloses a method according to claim 43, wherein retrieving information about a defect in the integrated circuit (IC) further comprises retrieving information that is generated by testing the integrated circuit (IC) to identify a defective circuit (inherent), and coding the information about the defect in the set of programmable elements (column 6, lines 12-13).

With regard to **claim 49**, Fuchigami discloses a method according to claim 48, wherein the integrated circuit (IC) comprises a programmable logic device. (As in the title, a memory is used which according to the specification of the applicant is used in a PLD.)

With regard to **claim 50**, Fuchigami discloses a method according to claim 49, wherein the defective circuit WL_n comprises a memory circuit MC within the programmable logic device (PLD).

15. Claims 28 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of Kalter et al (US Patent 5,796,662). (same reasons as the rejection of claim 51)

With regard to **claims 28 and 39**, Anand discloses a device which switches links 18 connected to blocks/columns of memory cells. Though he does not teach that the redundant circuitry comprises programmable logic circuitry, Anand does teach that Kalter is incorporated by reference and can be used in the column redundancy system. (see top of col. 4 of Anand)

Kalter teaches in figure 2, col. 4, lines 28-40 and col. 5, starting at line 33 that programmable logic arrays have been used with redundancy circuitry.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use programmable logic circuitry taught in Kalter with the redundancy system of Anand in order to properly correct errors in programmable logic.

16. Claims 28, 29, 39, and 40 are rejected (again) under 35 U.S.C. 103(a) as being unpatentable over Anand in view of Trimberger et al (US Patent 7,047,465).

Claims **28, 29, 39, and 40** specify that interconnect circuitry and programmable logic circuitry (which may or may not be present in Anand alone) may comprise the defective and redundant circuitry. Trimberger discusses (starting in col. 1 under "Background of the Invention") that memory cells may be coupled to programmable interconnect and programmable logic circuitry. The circuitry is adjusted according to this memory. The memory of Anand could logically be used as the memory cells with each

memory block, both normal and redundant, having associated programmable interconnect and programmable logic circuitry.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Anand and Trimberger in order to provide redundancy capabilities to a device comprising programmable logic and interconnects.

17. Claims 51 and 52 are rejected (again) under 35 U.S.C. 103(a) as being unpatentable over Anand in view of APA (as used above in the rejection of claim 50) and further in view of Trimberger et al (US Patent 7,047,465).

With regard to claims **51 and 52**, it would have been obvious to add the teachings of Trimberger to the combination of Anand and APA for similar reasons as claims 28, 29, 39, and 40 above to create the methods of claims 51 and 52.

Allowable Subject Matter

18. Claim 9-17 are allowed.

19. The following is a statement of reasons for the indication of allowable subject matter:

With regard to **claims 9-17**, the prior art does not teach or suggest, *in combination with the other limitations of the claims and as far as understood in view of 35 U.S.C. 112, 6th paragraph,* means for decoding the coded signals to generate decoded defect signals and for providing the decoded defect signals to means for storage of signals. In particular, figure 8 shows means for decoding 203 providing decoded defect signals (through lines 340) *in parallel to the PRESET inputs* of means

for storage (shift register composed of flip-flops 315 with scan chain input 325). The prior art teaches that the shift registers are loaded serially, not in parallel.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Weinberg whose telephone number is 571-272-6424. The examiner can normally be reached on M-F 9:00 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

mjw

HUAN HOANG
PRIMARY EXAMINER